FFmh: Metastable-Hardened Flip-Flops

In the late 1980s, Texas Instruments and other manufacturers developed SSI and MSI flip-flops that are specifically designed for board-level synchronizer applications. For example, the *74AS4374* was similar to the 74AS374, except that each individual flip-flop was replaced with a pair of flip-flops, as shown in Figure FFmh-1. Each pair of flip-flops could be used as a synchronizer of the type shown in Figure 8-76, so eight asynchronous inputs could be synchronized with one 74AS4374. The same approach is used in TI's 74ACT11478, a CMOS 8-bit register with pinouts different from the '374's.

74AS4374

The internal design of the 'AS4374 was improved to reduce τ and T_o compared to other 74AS flip-flops, but the biggest improvement in the 'AS4374 was a greatly reduced t_{setup}. Because the entire synchronizer of Figure 8-76 is built on a single chip, there are no input or output buffers between FF1 and FF2, and t_{setup} for FF2 is only 0.5 ns. Compared to a conventional 74AS flip-flop with a 5-ns t_{setup}, and assuming that $\tau = 0.40$ ns, this improves the MTBF by a factor of exp(4.5/.40), or about 77,000.

In recent years, the move toward faster CMOS technologies and higher integration has largely obsoleted specialized parts like the 'AS4374. As you can see from the last few rows in Table 8-43 on page 774, fast PLDs and CPLDs are available with values of τ that rival the fastest discrete devices while offering the convenience of integrating synchronization with many other functions. Still, the approach used by 'AS4374 is worth emulating in FPGA and ASIC designs. That is, whenever you have control over the layout of a synchronizer circuit, it pays to locate FF1 and FF2 as close as possible to each other and to connect them with the fastest available wires, in order to maximize the setup time available for FF2.

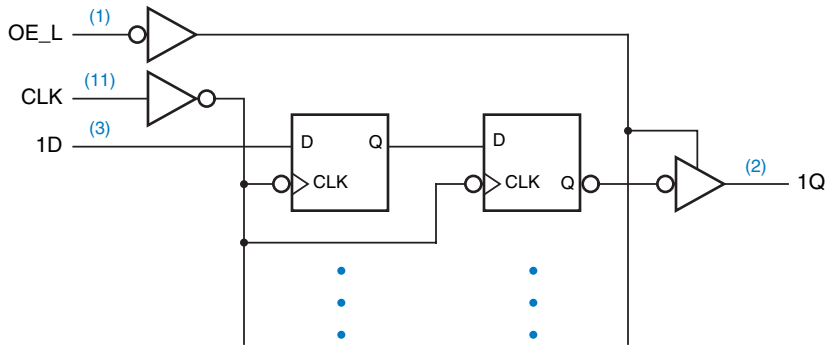

Figure FFmh-1
Logic diagram for the 74AS4374 octal dual-rank D flip-flop.