Sreg: Other MSI Shift Registers

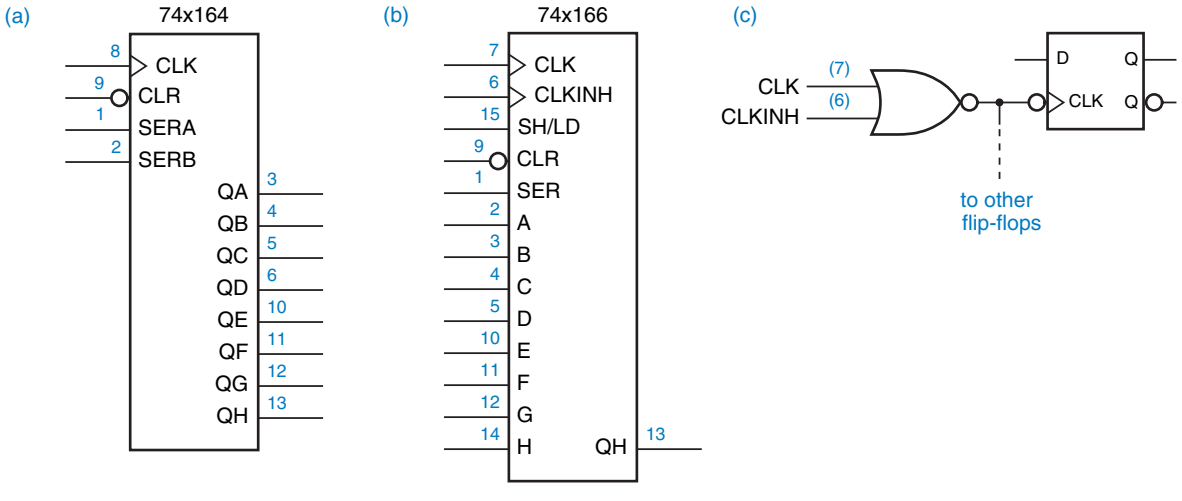
74x164

Figure Sreg-1 shows logic symbols for two MSI 8-bit shift registers. The *74x164* is a serial-in, parallel-out device with an asynchronous clear input (CLR_L). It has two serial inputs that are ANDed internally. That is, both SERA and SERB must be 1 for a 1 to be shifted into the first bit of the register.

74x166

The *74x166* is a parallel-in, serial-out shift register, also with an asynchronous clear input. This device shifts when SH/LD is 1 and loads new data otherwise. The ’166 has an unusual clocking arrangement called a “gated clock” (see also Section 8.8.2); it has two clock inputs that are connected to the internal flip-flops as shown in Figure Sreg-1(c). The designers of the ’166 intended for CLK to be connected to a free-running system clock, and for CLKINH to be asserted to inhibit CLK, so that neither shifting nor loading occurs on the next clock tick, and the current register contents are held. However, for this to work, CLKINH must be changed only when CLK is 1; otherwise, undesired clock edges occur on the internal flip-flops, causing extra shifts to occur. A much safer way of obtaining a “hold” function is employed in the 74x194 and in the next device that we discuss.

Figure Sreg-1 Traditional logic symbols for MSI shift registers: (a) 74x164 8-bit serial-in, parallel-out shift register; (b) 74x166 8-bit parallel-in, serial-out shift register; (c) equivalent circuit for 74x166 clock inputs.



The *74x299* is an 8-bit universal shift register in a 20-pin package; its symbol and logic diagram are given in Figures Sreg-2 and Sreg-3. The ’299’s functions and function table are similar to the ’194’s, as shown in Table Sreg-1. To save pins, the ’299 uses bidirectional three-state lines for input and output, as shown in the logic diagram. During load operations (S1 S0 = 11), the three-state drivers are disabled and data is loaded through the AQA–HQH pins. At other times the stored bits are driven onto these same pins if G1_L and G2_L are asserted. The leftmost and rightmost stored bits are available at all times on separate output-only pins, QA and QH.

Table Sreg-1 Function table for a 74x299 8-bit universal shift register.

	Inputs		*Next state*							
Function	***S1***	***S0***	***QA****	***QB****	***QC****	***QD****	***QE****	***QF****	***QG****	***QH****
Hold	0	0	QA	QB	QC	QD	QE	QF	QG	QH
Shift right	0	1	RIN	QA	QB	QC	QD	QE	QF	QG
Shift left	1	0	QB	QC	QD	QE	QF	QG	QH	LIN
Load	1	1	AQA	BQB	CQC	DQD	EQE	FQF	GQG	HQH

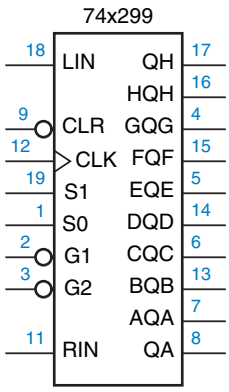


Figure Sreg-2 Traditional logic symbol for the 74x299.

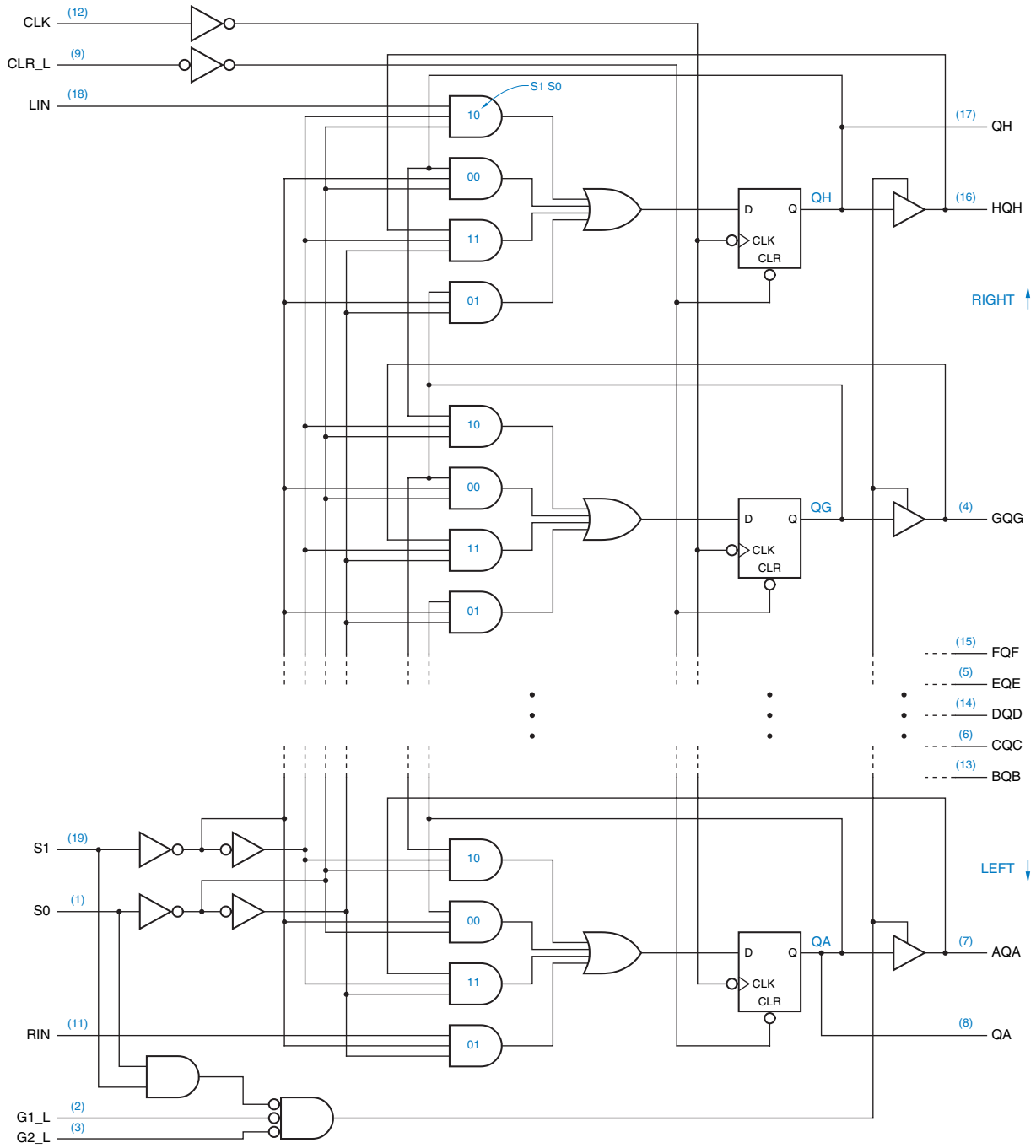


Figure Sreg-3 Logic diagram for the 74x299 8-bit universal shift register, including pin numbers for a standard 20-pin dual in-line package.

Exercises

Sreg.1 Write an ABEL program that provides the same functionality as a 74x299 shift register. Show how to fit this function into a single 22V10, or explain why it does not fit.